Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims

1. (currently amended): An apparatus comprising:

a host processing system comprising a non-volatile memory and a random access memory; and

a peripheral device comprising an intelligent I/O subsystem comprising a processing unit, said peripheral device also comprising a storage medium comprising machine-readable instructions stored thereon for initiating, by said peripheral device, an agent to reside on the host processing system, said agent capable of detecting a predetermined event in said host processing system, the agent comprising:

logic to modify an interrupt vector address to specify execution of machine-readable instructions at a location in the random access memory instead of at a location in the non-volatile memory; and

logic to initiate a reset procedure at the host processing system to commence execution of machine-readable instructions at the location in the random access memory in response to [[a]] said predetermined event at the host processing system.

2. (previously presented): The apparatus of claim 1, wherein the agent further comprises logic to load machine-readable instructions at the location in the random access memory for retrieving one or more programs from the storage medium of the peripheral device, the one or more programs comprising an operating system.

3. (cancelled).

4. (original): The apparatus of claim 2, wherein the one or more programs comprises a utility program and the agent further comprises logic to launch the utility program following a launch of the operating system in response to detection of the predetermined event.

5. (original): The apparatus of claim 1, wherein the predetermined event comprises an event at a user interface of the host processing system.

6. (original): The apparatus of claim 1, wherein the apparatus further comprises a data bus coupled between the host processing system and the peripheral device, and wherein the peripheral device further comprises logic for transmitting machine-readable instructions to the host processing system for creating the agent response to a procedure to enumerate the peripheral device on the bus.

7. (currently amended): A method comprising:

loading machine-readable instructions to a location in a random access memory of a host processing system, the host processing system comprising a non-volatile memory, the machine-readable instructions comprising machine-readable instructions to retrieve one or more programs from a peripheral device comprising an intelligent I/O subsystem comprising a processing unit, initiating, by said peripheral device, an agent to reside on said host processing system, said agent capable of detecting a predetermined event in said host processing system;

modifying, by said agent, an interrupt vector address to specify execution of machine-readable instructions at the location in the random access memory instead of at a location in the non-volatile memory; and

initiating, by said agent, a reset procedure at the host processing system to commence execution of machine-readable instructions in the location at the random access memory in response to a predetermined event at the host processing system.

8. (previously presented): The method of claim 7, wherein the one or more programs comprise an operating system and the method further comprises launching the operating system to the host processing system.

9. (cancelled)

10. (previously presented): The method of claim 8, wherein the one or more programs comprises a utility program and the method further comprises launching the utility program following a launch of the operating system in response to detection of the predetermined event.

11. (original): The method of claim 7, wherein the predetermined event comprises an event at a user interface of the host processing system.

12. (previously presented): The method of claim 7, wherein the method further comprises transmitting machine-readable instructions for modifying the interrupt vector address from the peripheral device to the host processing system through a data bus coupled between the host processing system and the peripheral device contemporaneously with a procedure to enumerate the peripheral device on the data bus.

13. (currently amended): An article comprising:

a storage medium comprising machine-readable instructions stored thereon for:

loading machine-readable instructions to a location in a random access memory of a host processing system, the host processing system comprising a non-volatile memory, the machine-readable instructions comprising machine-readable instructions to retrieve one or more programs from a peripheral device comprising an intelligent I/O subsystem comprising a processing unit, initiating, by said peripheral device, an agent to reside on said host processing system, said agent capable of detecting a predetermined event in said host processing system;

modifying, by said agent, an interrupt vector address to specify execution of machine-readable instructions at the location in the random access memory instead of at a location in the non-volatile memory; and

initiating, by said agent, a reset procedure at the host processing system to commence execution of machine-readable instructions in the location in the random access memory in response to a predetermined event at the host processing system.

14. (cancelled)

15. (previously presented): The article of claim 13, wherein the one or more programs comprise an operating system.

16. (cancelled)

17. (previously presented): The article of claim 15, wherein the one or more programs comprise a utility program and the storage medium further comprises machine-readable

instructions stored thereon to launch the utility program following a launch of the operating system in response to detection of the predetermined event.

18. (original): The article of claim 13, wherein the predetermined event comprises an event at a user interface of the host processing system.

19. (currently amended): A peripheral device comprising an intelligent I/O subsystem comprising a processing unit; logic to transmit machine-readable instructions to a host processing system through a data bus, the machine-readable instructions comprising instructions for ~~hosting of~~ initiating an agent on the host processing system, said agent capable of detecting a predetermined event in said host processing system, the agent comprising:

logic to modify an interrupt vector address to specify execution of machine-readable instructions at a location in a random access memory of the host processing system instead of at a location in a non-volatile memory of the host processing system ; and

logic to initiate a reset procedure at the host processing system to commence execution of machine-readable instructions in the location in the random access memory in response to a predetermined event at ~~the~~ said host processing system.

20. (original): The peripheral device of claim 19, the peripheral device further comprising:

an interface to a data bus for transmitting data to the data bus; and

logic to transmit the machine-readable instructions for hosting the agent to the host processing system contemporaneously with a procedure for enumerating the peripheral device on the data bus.

21. (currently amended): The peripheral device of claim 19, wherein the agent further comprises:

logic to load machine-readable instructions from the peripheral device to the location in the random access memory for one or more programs ~~comprise~~ comprising an operating system; and

logic to initiate a system reset procedure of the host processing system to launch the operating system to the host processing system in response to detection of the predetermined event.

22. (cancelled)

23. (original): The peripheral device of claim 21, wherein the one or more programs comprise a utility program and the agent further comprises logic to launch the utility program following a launch of the operating system in response to detection of the predetermined event.

24. (original): The peripheral device of claim 19, wherein the predetermined event comprises an event at a user interface of the host processing system.

25 – 30 (cancelled)

31. (previously presented): The apparatus of claim 1, wherein the non-volatile memory comprises a master boot record at the location in the non-volatile memory.

32. (previously presented): The apparatus of claim 31, wherein the location in the non-volatile memory corresponds with a cylinder-head-sector of the non-volatile memory.

33. (previously presented): The method of claim 7, wherein the non-volatile memory comprises a master boot record at the location in the non-volatile memory.

34. (currently amended): The ~~apparatus~~ method of claim 33, wherein the location in the non-volatile memory corresponds with a cylinder-head-sector of the non-volatile memory.

35. (previously presented): The article of claim 13, wherein the non-volatile memory comprises a master boot record at the location in the non-volatile memory.

36. (previously presented): The article of claim 35, wherein the location in the non-volatile memory corresponds with a cylinder-head-sector of the non-volatile memory.

37. (previously presented): The peripheral device of claim 19, wherein the non-volatile memory comprises a master boot record at the location in the non-volatile memory.

38. (previously presented): The apparatus of claim 37, wherein the location in the non-volatile memory corresponds with a cylinder-head-sector of the non-volatile memory.

39 – 40 (cancelled)